Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended and new claims added to more clearly claim Applicants invention. Support for the amended and newly drafted claims are found in the original claims and/or the Specification. No new matter has been added. For example new limitations in claim 1 are found in the specification beginning at line 5, page 13 and Figure 3:

"If the overlay registration measurement is not in accord with specification expectations, an overlay registration offset in accord with the block which corresponds with reference numeral 34 is revised. Such revision is typically effected incident to manual control."

CLAIM OBJECTIONS

Claims 1-7, 12-14, and 18-24 stand objected to for not clearly defining the term 'pilot lot'. The claims have been amended to more clearly define 'pilot' lot to overcome Examiners rejection.

Claims 18 and 19 have been amended to overcome Examiners rejection related to "lithography" process.

Claim Rejections under 35 USC 103(a)

Claims 1-28 stand rejected under 35 USC 103(a) as being unpatentable over Bode et al. (US 6,737,208) in view of Shimizu (US 6, 788,996).

Bode et al. disclose a process whereby a first photolithographically patterned layer is formed and then measured to determine an overlay registration error. Photolithographic process parameters are then adjusted in response to the overlay registration error **and a second photolithographic patterning process is carried out on a second photoresist layer formed on the same wafer (see Abstract).**

Thus, the method of Bode et al. is directed to correcting an overlay registration error with respect to forming **successively photolithographically patterned layers on a single wafer, thereby teaching away from a lot to lot process.** Bode et al., nowhere disclose the use of **pilot lots of substrates** as Applicants have disclosed and claimed for calibrating a photolithographic process prior to processing a subsequent lot of substrates according to the photolithographic process.

Thus, Bode et al. do not teach or disclose several aspects of Applicants disclosed and claimed invention, but rather teach away therefrom.

In addition to teaching away from processing **lots of substrates**, as Examiner notes, Bode et al. also fail to teach dividing one lot into a subset of lots (pilot lots) for use in calibrating a photolithographic process prior to processing a subsequent lot.

On the other hand, Shimizu teaches a process whereby plural wafers (substrates) in a lot are divided into a number of sublots corresponding **to different wafer manufacturing devices of the same kind** for processing the sublots **in parallel** (see Abstract; see col 2, lines 38-44)). The purpose of the invention is to reduce manufacturing time in a production line. Nowhere does Shimizu disclose a calibration process prior to processing substrates.

There is no apparent motivation for combining the single **wafer-to-wafer overlay registration correction method** of Bode et al. with the method of Shimizu **for parallel processing of sublots of wafers to reduce manufacturing time.** Nevertheless, assuming *arguendo*, a proper motivation for such combination, such

combination does not produce Applicants disclosed and claimed invention.

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123, USPQ 349 (CCPA 1959).*

"A prior art reference must be considered in its entirety, i.e., as a whole including portions that would lead away from the claimed invention." *W.L. Gore & Associates, Inc., Garlock, Inc., 721 F.2d, 1540, 220 USPQ 303 (Fed Cir. 1983), cert denied, 469 U.S. 851 (1984).*

Since the cited references are insufficient to make out a *prima facie* case of obviousness with respect to Applicants independent claims, neither has a *prima facie* case been made out with respect to Applicants dependent claims.

The Claims have been amended to clarify Applicants' disclosed and claimed invention. A favorable reconsideration of Applicants' claims is respectfully requested.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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